WHAT IS CLAIMED IS:

1. A data storage device comprising:

write-once memory;

non-volatile memory; and

a circuit for writing user data to the write-once memory and storing in the non-volatile memory at least one of the user data and error correction data.

2. The device of claim 1, wherein the circuit stores an incomplete block of user data in the non-volatile memory; and uses the stored user data to form a full block when new user data is received; and wherein the circuit generates error correction data for the full block, and writes the full block of user data and the error correction data to the write-once memory.

3. The device of claim 1, wherein the circuit writes an incomplete block of user data to the write-once memory, generates error correction data for a full block including the user data and padding, and stores at least some of the error correction data in the non-volatile memory.

4. The device of claim 3, wherein final error correction data is written to the write-once memory and temporary error correction data is written to the non-volatile memory.

5. The device of claim 3, wherein the incomplete block of user data is written between starting and ending addresses in the write-once memory; and wherein the circuit also writes the ending address to the non-volatile memory.

6. The device of claim 3, wherein the circuit accesses the incomplete block from the write-once memory, pads the incomplete block, accesses the error

correction data, and uses the error correction data to perform error correction on the padded block.

7. The device of claim 6, wherein the device receives new user data, and adds the new user data to the error-corrected user data.

8. The device of claim 3, wherein the error correction data includes RS-PC code words.

9. The device of claim 1, wherein storage capacity of the non-volatile memory is less than full user data block size.

10. A data storage device comprising:

a substrate;

at least one level of solid state one-time programmable memory on the substrate;

non-volatile memory in the substrate; and

a circuit for writing user data to the write-once memory and using the user data to create error correction data, at least some of the error correction data stored in the non-volatile memory.

11. The device of claim 10, wherein the circuit writes an incomplete block of user data to the write-once memory, generates error correction data for a full block including the incomplete block and padding, and stores the error correction data in the non-volatile memory.

12. The device of claim 11, wherein final error correction data is written to the write-once memory and temporary error correction data is written to the non-volatile memory.

13. The device of claim 11, wherein the incomplete block of user data is written between starting and ending addresses in the write-once memory; and wherein the circuit also writes the ending address to the non-volatile memory.

14. The device of claim 11, wherein the circuit accesses the incomplete block from the write-once memory, accesses the error correction data from the non-volatile memory, pads the incomplete block, and uses the error correction data to perform error correction on the padded block.

15. The device of claim 14, wherein the device receives new user data, and adds the new user data to the error-corrected user data.

16. The device of claim 10, wherein the error correction data includes RS-PC code words.

17. Apparatus comprising:

write-once memory;

means for buffering an incomplete block of user data;

means for storing the incomplete block in the write-once memory;

means for adding padding to the incomplete block to form a padded block;

means for generating error correction data for the padded block; and

means for storing at least some of the error correction data in the non-volatile memory.

18. Apparatus for a data storage device including write-once memory and non-volatile memory, the apparatus comprising a control circuit for writing user data to the write-once memory and storing in the non-volatile memory at least one of the user data and the error correction data.

19. The apparatus of claim 18, wherein the circuit writes an incomplete block of user data to the write-once memory, generates error correction data for

a full block including the user data and padding, and stores at least some of the error correction data in the non-volatile memory.

20. The apparatus of claim 19, wherein final error correction data is written to the write-once memory and temporary error correction data is written to the non-volatile memory.

21. The apparatus of claim 19, wherein the incomplete block of user data is written between starting and ending addresses in the write-once memory; and wherein the circuit also writes the ending address to the non-volatile memory.

22. The apparatus of claim 19, wherein the circuit accesses the incomplete block from the write-once memory, accesses the error correction data, and uses the error correction data to perform error correction on the user data in the incomplete block.

23. The apparatus claim 22, wherein the device receives new user data, and adds the new user data to the error-corrected user data.

24. A method of writing to a device including non-volatile memory and write-once memory, the method comprising:

buffering an incomplete block of user data;

storing the incomplete block in the write-once memory;

adding padding to the incomplete block to form a padded block;

generating error correction data for the padded block; and

storing at least some of the error correction data in the non-volatile memory.

25. The method of claim 24, wherein the incomplete block of user data is written between starting and ending addresses in the write-once memory; and

wherein the method further comprises writing the ending address to the non-volatile memory.

26. The method of claim 25, further comprising:

accessing the incomplete block from the write-once memory;

accessing the error correction data;

padding the incomplete block; and

using the error correction data to perform error correction on the padded block.

27. The method of claim 26, further comprising:

receiving new user data;

adding the new user data to the corrected user data to form a full block,

generating new error correction data for the full block; and

writing the new error correction data and the new user data to the write-once memory.